

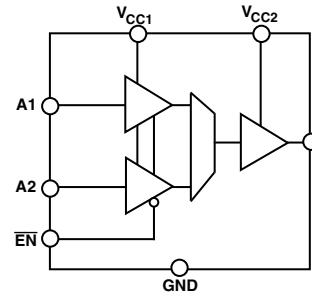
FEATURES

Operates from 1.65 V to 3.6 V Supply Rails
 Unidirectional Signal Path, Bidirectional Level Translation
 Tiny 8-Lead SOT-23 Package
 Short Circuit Protection
 LVTTTL/CMOS Compatible Inputs

APPLICATIONS

Level Translation
 Low Voltage ASIC Translation
 Low Voltage Clock Switching
 Serial Interface Translation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG3232 is a level translator 2-1 mux designed on a sub-micron process and operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, i.e., it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may flow only from A to Y.

This type of device may be used in applications requiring communication between devices operating from different supply levels.

The level translator mux is packaged in one of the smallest footprints available for its pin count. The 8-lead SOT-23 package requires only 8.26 mm × 8.26 mm of board space.

PRODUCT HIGHLIGHTS

1. Bidirectional level translation matches any voltage level from 1.65 V to 3.6 V.
2. The device offers high performance and is fully guaranteed across the supply range.
3. Short circuit protection.
4. Tiny SOT-23 package.

Table I. Truth Table

$\overline{\text{EN}}$	Function
L	A1-Y
H	A2-Y

*Patent Pending

REV. A

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ADG3232—SPECIFICATIONS¹ ($V_{CC1} = V_{CC2} = 1.65\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$. All specifications T_{MIN} to T_{MAX} , unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ ²	Max	Unit
LOGIC INPUTS/OUTPUTS³						
Input High Voltage ⁴	V_{IH}	$V_{CC1} = 3.0\text{ V to }3.6\text{ V}$	1.35			V
	V_{IH}	$V_{CC1} = 2.3\text{ V to }2.7\text{ V}$	1.35			V
	V_{IH}	$V_{CC1} = 1.65\text{ V to }1.95\text{ V}$	$0.65 V_{CC}$			V
Input Low Voltage ⁴	V_{IL}	$V_{CC1} = 3.0\text{ V to }3.6\text{ V}$			0.80	V
	V_{IL}	$V_{CC1} = 2.3\text{ V to }2.7\text{ V}$			0.70	V
	V_{IL}	$V_{CC1} = 1.65\text{ V to }1.95\text{ V}$			$0.35 V_{CC}$	V
Output High Voltage	V_{OH}	$I_{OH} = -100\text{ mA}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$	2.4			V
		$V_{CC2} = 2.3\text{ V to }2.7\text{ V}$	2.0			V
		$V_{CC2} = 1.65\text{ V to }1.95\text{ V}$	$V_{CC} - 0.45$			V
		$I_{OH} = -4\text{ mA}$, $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$	2.0			V
		$V_{CC2} = 1.65\text{ V to }1.95\text{ V}$	$V_{CC} - 0.45$			V
Output Low Voltage	V_{OL}	$I_{OH} = -8\text{ mA}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$	2.4			V
		$I_{OH} = +100\text{ mA}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$			0.40	V
		$V_{CC2} = 2.3\text{ V to }2.7\text{ V}$			0.40	V
		$V_{CC2} = 1.65\text{ V to }1.95\text{ V}$			0.45	V
		$I_{OH} = +4\text{ mA}$, $V_{CC2} = 2.3\text{ V to }2.7\text{ V}$			0.40	V
		$V_{CC2} = 1.65\text{ V to }1.95\text{ V}$			0.45	V
		$I_{OH} = +8\text{ mA}$, $V_{CC2} = 3.0\text{ V to }3.6\text{ V}$			0.40	V
SWITCHING CHARACTERISTICS^{4, 5}						
Propagation Delay, t_{PD}						
A1 to Y	t_{PHL}, t_{PLH}	$3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		4	6.5	ns
A2 to Y	t_{PHL}, t_{PLH}	$3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		3.5	5.4	ns
A1 to Y	t_{PHL}, t_{PLH}	$2.5\text{ V} \pm 0.2\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		5	7.2	ns
A2 to Y	t_{PHL}, t_{PLH}	$2.5\text{ V} \pm 0.2\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		4.5	6.5	ns
A1 to Y	t_{PHL}, t_{PLH}	$1.8\text{ V} \pm 0.15\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		6.5	10.25	ns
A2 to Y	t_{PHL}, t_{PLH}	$1.8\text{ V} \pm 0.15\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		6.5	10	ns
ENABLE Time \overline{EN} to Y	t_{EN}	$3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		4.5	6.5	ns
DISABLE Time \overline{EN} to Y	t_{DIS}	$3.3\text{ V} \pm 0.3\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		4	6.5	ns
ENABLE Time \overline{EN} to Y	t_{EN}	$2.5\text{ V} \pm 0.2\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		5	7.7	ns
DISABLE Time \overline{EN} to Y	t_{DIS}	$2.5\text{ V} \pm 0.2\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		4.8	7.2	ns
ENABLE Time \overline{EN} to Y	t_{EN}	$1.8\text{ V} \pm 0.15\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		7	12	ns
DISABLE Time \overline{EN} to Y	t_{DIS}	$1.8\text{ V} \pm 0.15\text{ V}$, $C_L = 30\text{ pF}$, $V_T = V_{CC}/2$		6.5	10.5	ns
Input Leakage Current	I_I	$0 \leq V_{IN} \leq 3.6\text{ V}$			± 1	μA
Output Leakage Current	I_O	$0 \leq V_{IN} \leq 3.6\text{ V}$			± 1	μA
POWER REQUIREMENTS						
Power Supply Voltages	V_{CC1}		1.65		3.6	V
	V_{CC2}		1.65		3.6	V
Quiescent Power Supply Current	I_{CC1}	Digital Inputs = 0 V or V_{CC}			2	μA
	I_{CC2}	Digital Inputs = 0 V or V_{CC}			2	μA
Increase in I_{CC} per Input	ΔI_{CC12}	$V_{CC} = 3.6\text{ V}$, One Input at 3.0 V; Others at V_{CC} or GND			0.75	μA

NOTES

¹ Temperature range is as follows: B Version, -40°C to $+85^\circ\text{C}$.

² All typical values are at $V_{CC1} = V_{CC2}$, $T_A = 25^\circ\text{C}$, unless otherwise stated.

³ V_{IL} and V_{IH} levels are specified with respect to V_{CC1} ; V_{OH} and V_{OL} levels are with respect to V_{CC2} .

⁴ Guaranteed by design, not subject to production test.

⁵ See Test Circuits and Waveforms.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

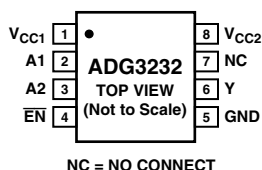
(T_A = 25°C, unless otherwise noted.)

V _{CC} to GND	−0.3 V to +4.6 V
A1, $\overline{\text{EN}}$ Input Voltage	−0.3 V to +4.6 V
A2	−0.3 V to V _{CC1} to +0.3 V
DC Output Current	25 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

8-Lead SOT-23	
θ_{JA} Thermal Impedance	211°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature (<20 sec)	235°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3232 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



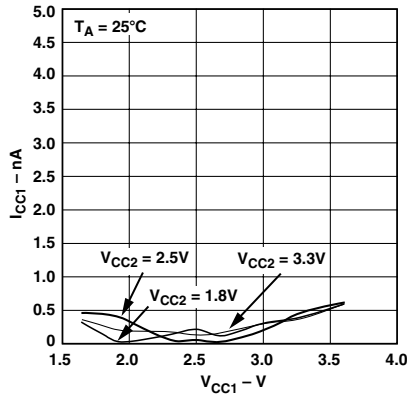
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG3232BRJ-REEL	−40°C to +85°C	SOT-23	RJ-8	W3B
ADG3232BRJ-REEL7	−40°C to +85°C	SOT-23	RJ-8	W3B

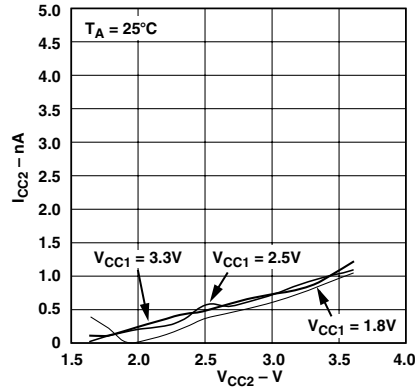
PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	V _{CC1}	Supply Voltage 1 can be any supply voltage from 1.65 V to 3.6 V.
2	A1	Input Referred to V _{CC1} .
3	A2	Input Referred to V _{CC1} .
4	$\overline{\text{EN}}$	Active Low Device Enable. When low, bypass mode is enabled; when high, the device is in normal mode.
5	GND	Device Ground Pin.
6	Y	Output Referred to V _{CC2} .
7	NC	Not Internally Connected.
8	V _{CC2}	Supply Voltage 2 can be any supply voltage from 1.65 V to 3.6 V.

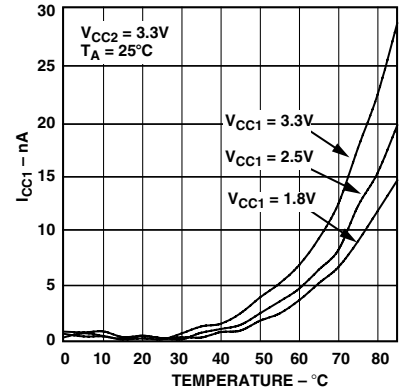
ADG3232—Typical Performance Characteristics



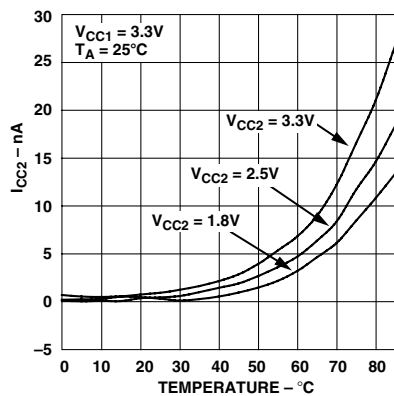
TPC 1. I_{CC1} vs. V_{CC1}



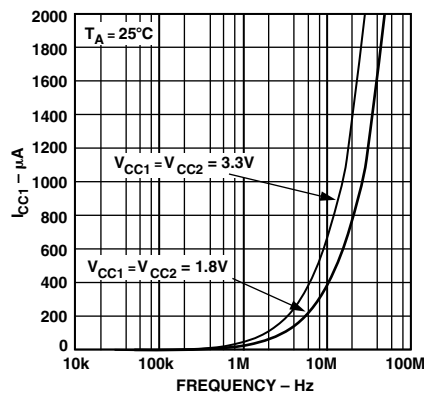
TPC 2. I_{CC2} vs. V_{CC2}



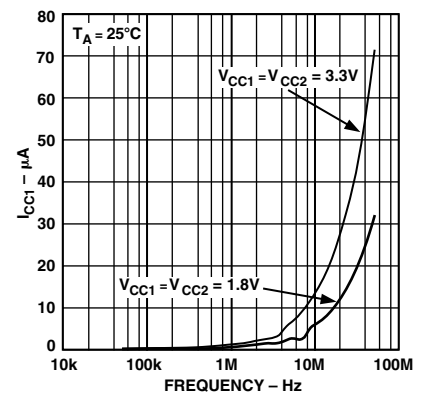
TPC 3. I_{CC1} vs. Temperature



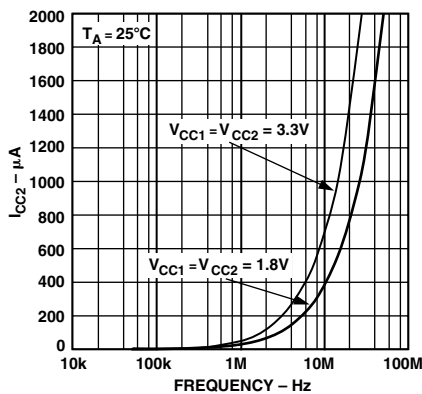
TPC 4. I_{CC2} vs. Temperature



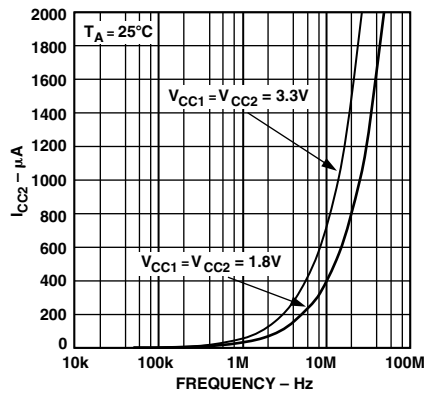
TPC 5. I_{CC1} vs. Frequency, A1-Y



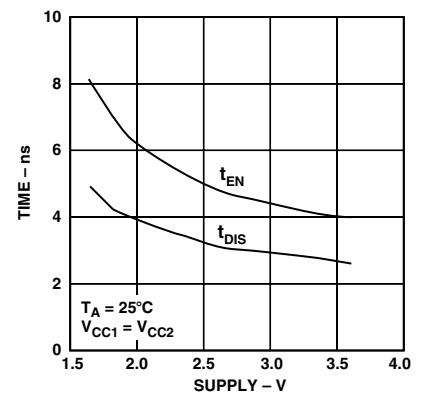
TPC 6. I_{CC1} vs. Frequency, A2-Y



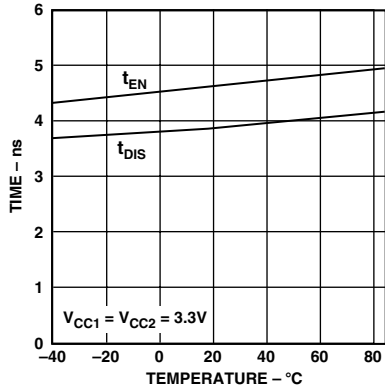
TPC 7. I_{CC2} vs. Frequency, A1-Y



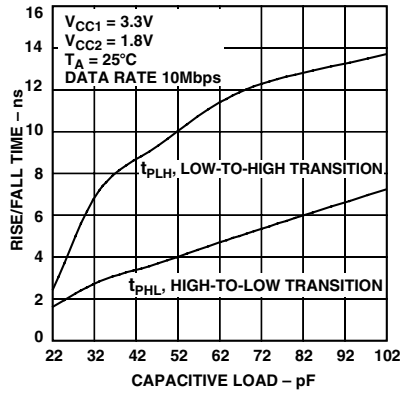
TPC 8. I_{CC2} vs. Frequency, A2-Y



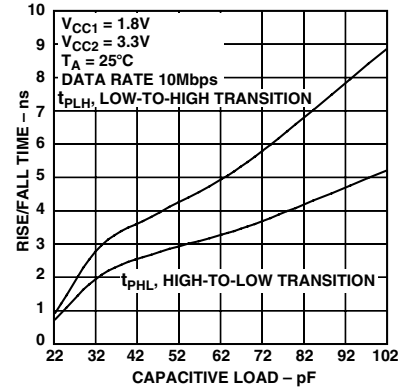
TPC 9. Enable, Disable Time vs. Supply



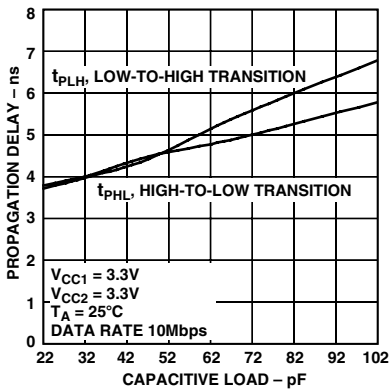
TPC 10. Enable, Disable Time vs. Temperature



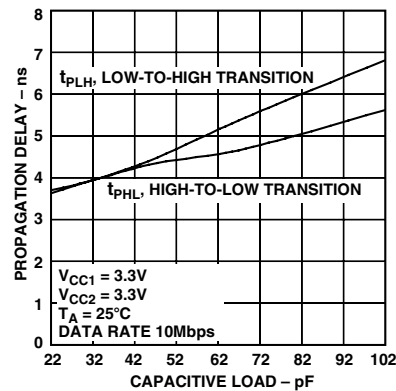
TPC 11. Rise/Fall Time vs. Capacitive Load, A1/A2-Y



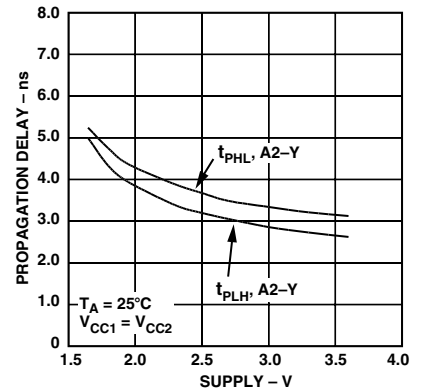
TPC 12. Rise/Fall Time vs. Capacitive Load, A1/A2-Y



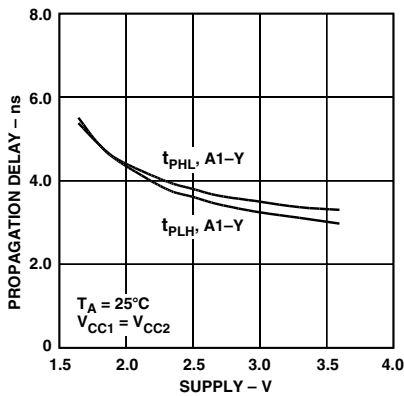
TPC 13. Propagation Delay vs. Capacitive Load, A2-Y



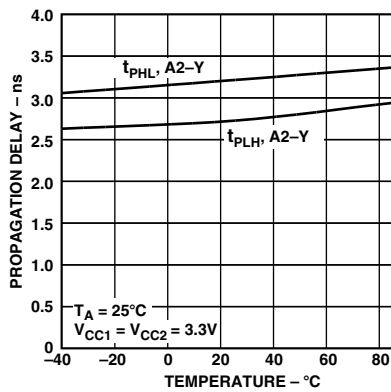
TPC 14. Propagation Delay vs. Capacitive Load, A1-Y



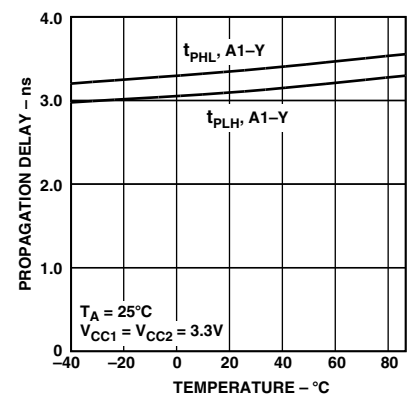
TPC 15. Propagation Delay vs. Supply



TPC 16. Propagation Delay vs. Supply, A1-Y

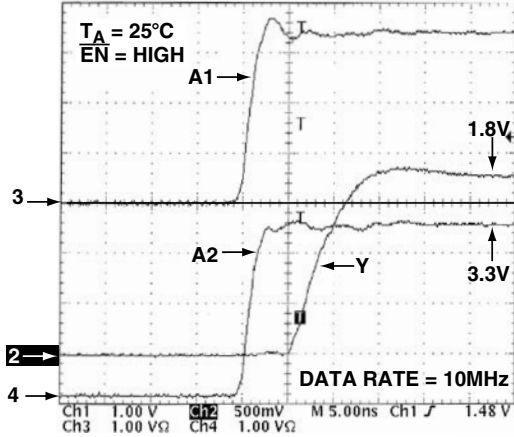


TPC 17. Propagation Delay vs. Temperature

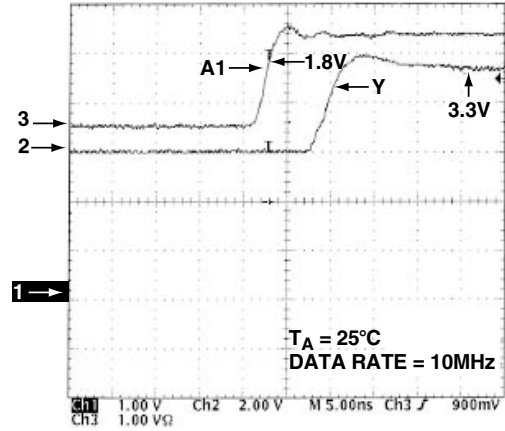


TPC 18. Propagation Delay vs. Temperature, A1-Y

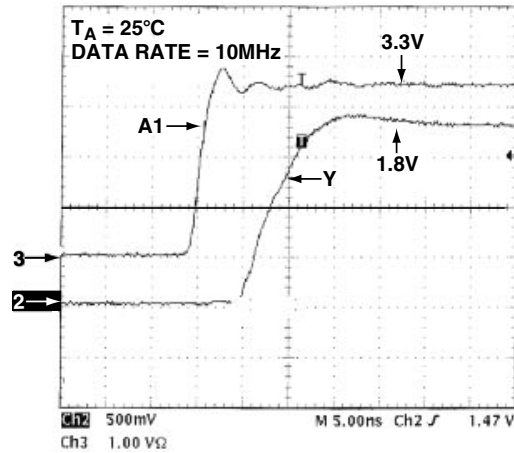
ADG3232



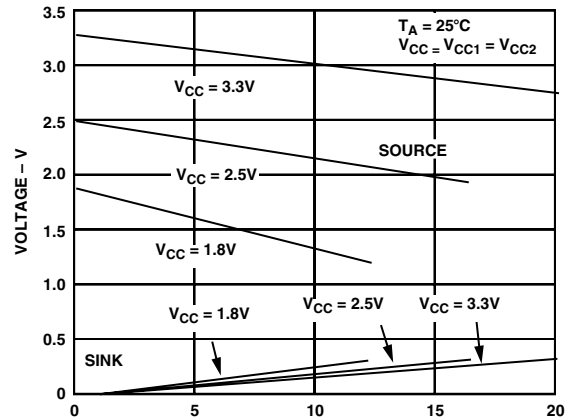
TPC 19. Input/Output $V_{CC1} = 3.3V, V_{CC2} = 1.8V$



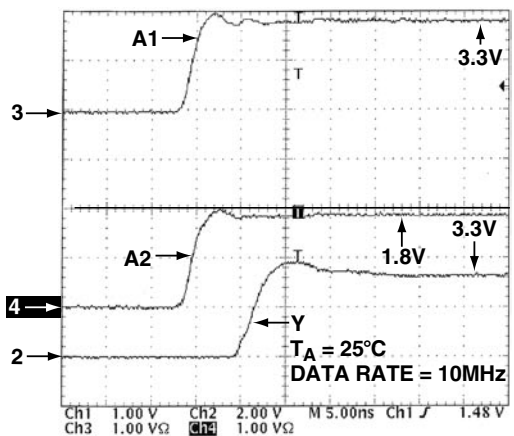
TPC 22. Input/Output $V_{CC1} = 3.3V, V_{CC2} = 1.8V$



TPC 20. Input/Output $V_{CC1} = 1.8V, V_{CC2} = 3.3V$



TPC 23. Y Sink and Source Current



TPC 21. Input/Output $V_{CC1} = 1.8V, V_{CC2} = 3.3V$

TEST CIRCUITS

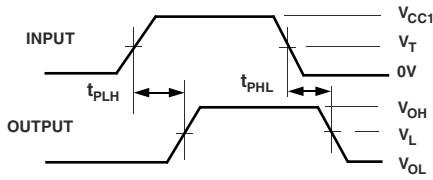


Figure 1. Propagation Delay

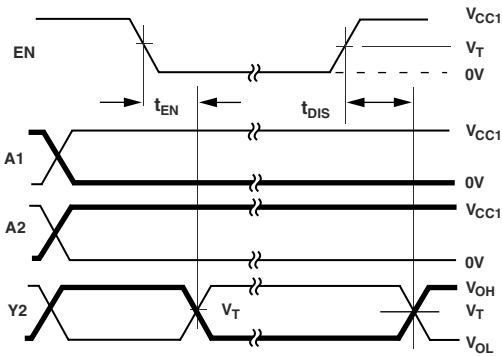


Figure 2. Enable and Disable Times

DESCRIPTION

The ADG3232 is a mux level translating device designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, i.e., it translates lower voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A to Y.

A1 and EN Input

The A1 and enable (EN) inputs have V_{IL}/V_{IH} logic levels so that the part can accept logic levels of V_{OL}/V_{OH} independent of the value of the supply being used. Both these inputs (A1 and EN) are capable of accepting inputs outside the V_{CC1} supply range. There are no internal diodes to the supply rails on these pins, so they can handle inputs above the supply but inside the absolute maximum ratings.

Operation

Figure 3 shows the ADG3232 in a typical application; the signal paths are from A1 or A2 to Y. The device will level translate the signal applied to A1/A2 from a V_{CC1} logic level (this level translation can be either to a higher or a lower supply) and route the signal to the Y output, which will have standard V_{OL}/V_{OH} levels for V_{CC2} supplies.

The supplies in Figure 3 may be any combination of supplies, e.g., V_{CC1} and V_{CC2} may be anywhere in the 1.65 V to 3.6 V range.

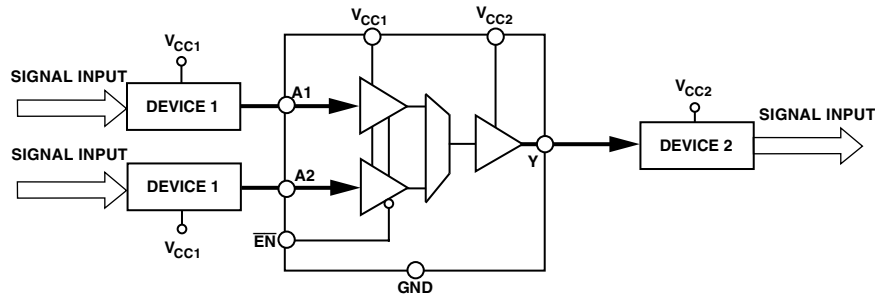
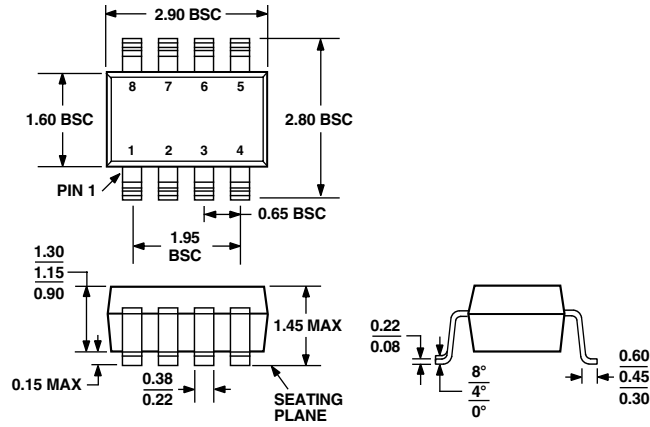


Figure 3. Typical Operation of the ADG3232 Level Translating Switch

OUTLINE DIMENSIONS

8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-178BA

C03299-0-7/03(A)

Revision History

Location	Page
7/03—Data Sheet changed from REV. 0 to REV. A.	
Change to PIN FUNCTION DESCRIPTIONS	3